A 94-GHz 130-mW InGaAs/InAlAs/InP HEMT High-Power MMIC Amplifier

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Abstract—**We have developed W-band high-power monolithic microwave integrated circuit (MMIC) amplifiers using passivated 0.15-μm gate length InGaAs/InAlAs/InP HEMT's. A 640-μm single-stage MMIC amplifier demonstrated an output power of 130 mW with 13% power-added efficiency and 4-dB associated gain at 94 GHz. This result represents the best output power to date measured from a single fixtured InP-based HEMT MMIC at this frequency.**

I. Introduction

RECENT years have seen intensive development of monolithic microwave integrated circuit (MMIC) power amplifiers using the GaAs-based AlGaAs/InGaAs pseudomorphic HEMT's (PHEMT's) [1]–[6] and InP-based InAlAs/InGaAs HEMT's [7] for applications at 94 GHz. InP-based InAlAs/InGaAs HEMT's have demonstrated the best gain and lowest noise figure for any three-terminal solid-state device [8], [9] due to their superior transport properties. Very-high-gain InP HEMT MMIC LNA's have been realized at frequencies as high as 140 GHz [8]. Because of its high gain, the InP HEMT has also demonstrated higher power-added efficiency (PAE) than GaAs-based PHEMT for the same output power level at 94 GHz [7], even though the former has lower breakdown voltages.

Because of the relative immaturity of InP HEMT development, the reported output power of InP HEMT amplifiers has been limited to about 50 mW [7], [10]. In this paper, we report a 640-μm single-stage InP HEMT MMIC amplifier that delivered 130-mW output power with 13% PAE at 94 GHz. This result represents the best output power fixture data to date measured from a single InP-based HEMT MMIC at this frequency.

II. Device and MMIC Optimization and Fabrication

The inset of Fig. 1 shows the schematic of our 0.15-μm gate-length, double-doped, double heterostructure InP HEMT. To achieve state-of-the-art performance, we have improved the delta doping density, ohmic contact layer, substrate thickness, and compact device layout as reported previously [7]. Further optimization in gate recess process has enabled us to achieve the best results. We have been targeting $V_{\rm gp}$ (the gate voltage where peak g_m occurs) at -0.1 to -0.15 V. This results in a typical g_m of 700 mS/mm, as compared to 1000 mS/mm in our low-noise HEMT, which is etched deeper and has a $V_{\rm gp}$ of $\sim$+0.2 V. The current–voltage characteristics of a 0.15-μm gate-length InP power HEMT are shown in Fig. 1. The small-signal equivalent circuit parameters of a 8-finger 160-μm device are listed in Table I.

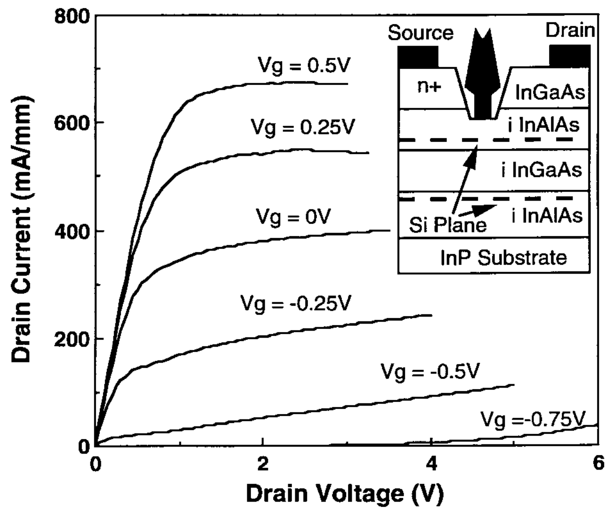

Fig. 1. Current–voltage characteristics of a double heterostructure 0.15-μm gate InGaAs-InAlAs-InP power HEMT. The inset shows a schematic of the device cross section.

TABLE I
Small-Signal Equivalent Circuit Parameters of an 8-Finger 0.15-μm Gate InP HEMT with 160-μm Total Gate Periphery

Lg	0.018 nH	gm	0.15 S
Ld	0.012 nH	Rds	165 Ω
Ls	0.0005 nH	τ	0.15 ps
Rg	2.5 Ω	Cgd	0.015 pF
Rd	1.1 Ω	Cds	0.038 pF
Rs	0.9 W	Ri	0.1 Ω

The amplifier circuits were fabricated using TRW's established InP HEMT MMIC process [11], [12]. We used 2-mil-thin substrates, which allowed us to reduce the size of the via holes and place them closer to the source. This not only lowers parasitic source inductance, but also offers improved thermal conductivity.

The picture of a 640-μm single-stage amplifier is shown in Fig. 2. Quarter-wave open stubs are used for RF bypass

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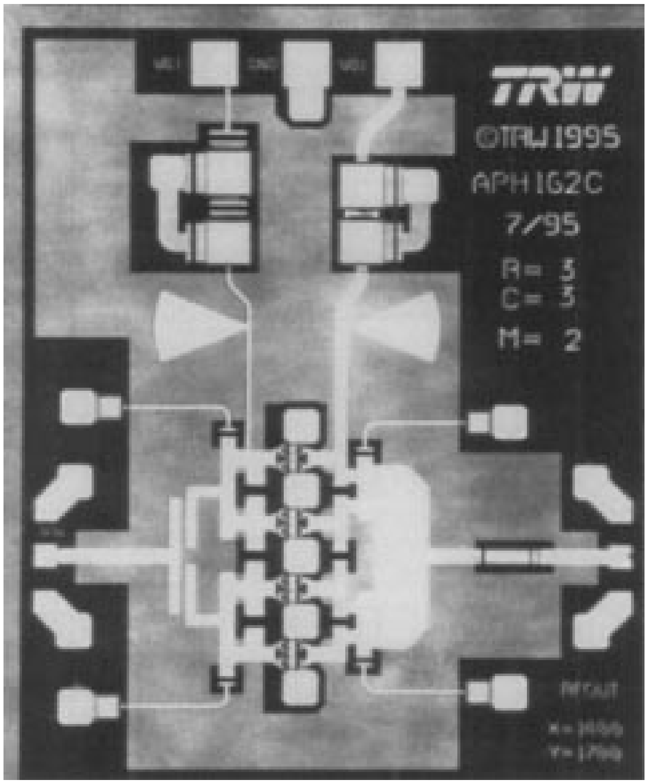
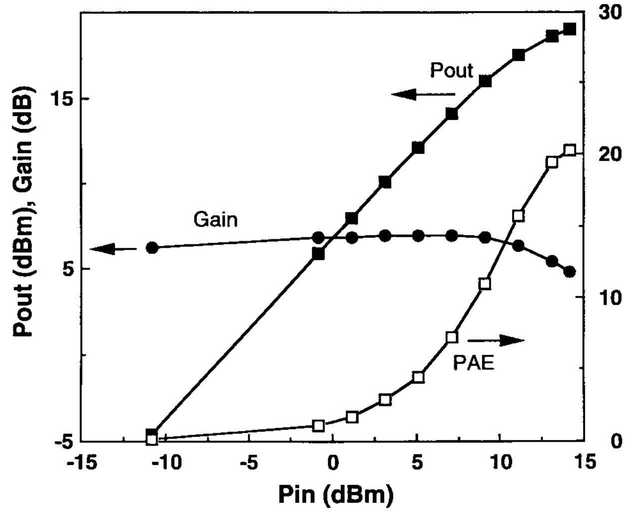


Fig. 2. Picture of a single-stage 94-GHz 0.15-μm $\times$ 640-μm InP HEMT MMIC power amplifier.

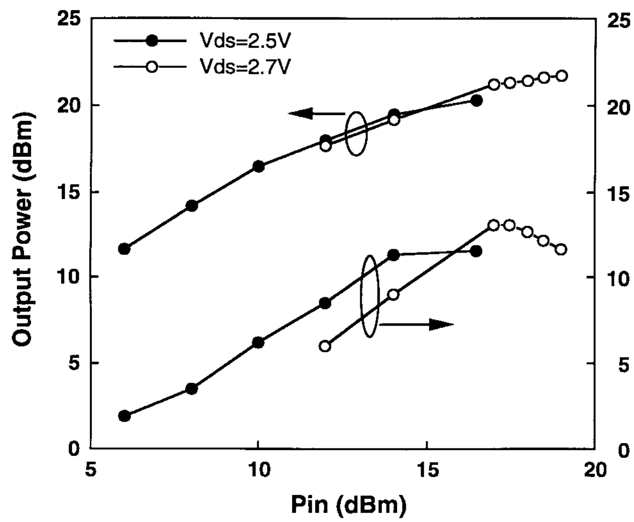
to isolate the bias circuitry from the RF matching networks. The input matching network, which utilizes coupled-lines, as well as the series R-C shorted quarter-wave stubs at both the input and output, are used to enhance out-of-band stability. The most significant parameter affecting output power is the matching impedance at the amplifier output. We derived the output match for the amplifier based on harmonic balance simulations using our in-house-developed nonlinear model. Rigorous design and analysis methodology, including accurate device modeling and full-wave electromagnetic (EM) simulation of passive structures, ensured the optimization of gain and bandwidth.

III. Results and Discussions

The MMIC's were diced and mounted on test fixtures for power and efficiency evaluation. The waveguide-to-microstrip end-to-end insertion loss was measured to be 1.7 dB at 94 GHz. This loss was corrected from the measurement results. Two single-stage MMIC amplifiers of 320-μm and 640-μm total gate periphery, respectively, were characterized. The 320-μm MMIC amplifier consists of two microcells, each with eight fingers with 20-μm gate width per finger. The MMIC demonstrated an output power of 80 mW with 4.9-dB associated gain and 20.2% power-added efficiency (PAE) [Fig. 3(a)] at $V_{\rm ds} = 2.5$ V. This result surpasses our previous in-fixture measurement data of 54 mW with 20% PAE and represents a new milestone of the best fixture data of efficiency and output power.



(a)



(b)

Fig. 3. Output power and PAE of (a) 320-μm gate width and (b) 640-μm gate width single-stage InP HEMT power amplifiers measured at 94 GHz.

The 640-μm single-stage MMIC amplifier consists of four 8-finger, 160-μm microcells. When biased at a $V_{\rm ds}$ of 2.7 V, it delivers an output power of 130 mW with 13% PAE and 4-dB associated gain as shown in Fig. 3(b). To our knowledge, this is the highest power ever achieved from a single InP-based HEMT MMIC amplifier at 94 GHz.

We attribute the improved power performance to optimized gate recess depth. Gate recess depth is an important variable in process optimization due to the trade-off between $I_{\max}$ and g_m. The gate recess depth can be optimized by referencing to $V_{\rm gp}$ as measured after gate metallization. We have systematically investigated the relationship between $V_{\rm gp}$ and power performance for a single-stage MMIC amplifier with 320-μm total gate periphery. The output power data were measured in-fixture at 94 GHz with input power levels such that the power gain was 4 dB. The dc bias conditions were optimized for maximum output power. We found that as we changed $V_{\rm gp}$ from $+0.25$ V to -0.13 V by varying recess depth, device peak g_m dropped from 900 to 680 mS/mm, but

$I_{\max}$ increased from 450 to 650 mA/mm. The single-stage amplifier output power also increased from 12.5 to >20 dBm. A similar trend was observed from an amplifier with 160-μm total gate periphery and different matching network. The improved power performance of the negative $V_{\rm gp}$ device is due to the increased $I_{\max}$. Although the g_m of the negative $V_{\rm gp}$ device is lower, its amplifier power gain is still comparable to that of positive $V_{\rm gp}$ device at 94 GHz.

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